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09/727,393	11/29/2000	Allen P. Chen	10559-385001/P10191	4146

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EXAMINER	
SEFCHECK, GREGORY B	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,393	CHEN ET AL.	
	Examiner	Art Unit	
	Gregory B Sefcheck	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Request for Continued Examination filed 2/10/2005 is acknowledged.
- Claims 1, 3, 7, 9, 21, 24, 29, and 32 are amended.
- Claims 1-34 remain pending.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 9 and 24 are objected to because of the following informalities:

   - Claims 9 and 24 both make reference to a "port polling process". The proper antecedent basis for this reference has been deleted in the amendment.

   Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 3, 9, 10, 11, 18, 19, 24, 26, 27, and 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam et al. (US006671758B1), hereafter Cam.

- In regards to Claims 1, 2, 9, 10, 18, 19, 24, 26, 27, and 32,

Cam discloses a packet data transfer method on an interface having a large number of ports (Abstract; claim 1 – intra-packet switching method).

Referring to Fig. Cam shows that a Layer/master device 22 polls the PHY devices 14-20 to determine which have data waiting to be transferred (Col. 1, lines 38-41; claim 1,9,24,32 – determining which ports contain a data packet available for processing).

Cam shows that data packets waiting to be transferred from polled PHY devices are fragmented to a maximum block size (cell) of data. This maximum block size may be fixed at start-up or by programming through an external management interface (Col. 3, lines 2-9; claim 1,9,24,32 – fragmenting available data packet into at least one cell having defined size; claim 1,9,24,26,32 – fragmentation continues until a user-defined number of cells are generated; claim 2,10,27 – monitoring the number of cells produced to determine if user-defined number are generated; claim 18,19 – user interface for allowing user to specify user-defined cells to be generated by packet fragmentation process).

Referring to Fig. 6, Cam further discloses that a selected PHY device transfers a block of fragmented packet data upon selection and deselects itself at the end of its

transfer period, which is set at the specified maximum block size, and the next PHY with data to transmit is selected (Col. 12-13, lines 63-16).

However, Cam does not explicitly disclose the fragmentation process where a portion of a second available data packet on a different port is fragmented subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet.

Referring to Figs. 5 and 11, Cam shows that packets awaiting transfer from multiple PHY devices will be transferred a maximum block size at a time before deselecting itself, at which point the next PHY device begins transfer of a maximum block size. In the situation where the PHY devices have large packets to be transferred, a first portion of the packet on the first PHY will be fragmented and transferred, followed by a first portion of a second packet on the second PHY being fragmented and transferred. Subsequent portions of the first packet at the first PHY would be fragmented and transferred at its next selected transfer period (claim 1,9,24,26,32 - fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of Cam by fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet. Such an implementation would enable the method of Cam to process large

packets at multiple PHY devices such that no one PHY device starves bandwidth from the other PHY devices.

- In regards to Claims 3 and 11,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Referring to Fig. 5, Cam shows that polling of the PHY devices to determine if packets are available for processing is continuously done so that it is determined if any other ports contain packets available for processing other than those that have already so indicated (Col. 1, lines 38-41; Col. 3, lines 19-24; claim 3,11 – re-determining if packets are available for processing on any of the plurality of ports if the number of cells have been generated from the first port determined to have a packet available).

- In regards to Claims 29-31 and 33,

Cam discloses a packet data transfer process that covers all limitations of claim 29 similar to claims 1, 9, 24, and 32 as shown above.

Cam does not explicitly show implementing the methods and processes through computer programs residing on computer readable medium such as read-only and random access memory in which the processor and memory are on a single board computer.

It is well known that software implementation by a computer having a processor and memory for performing process/method functions can be cost efficient and enable

accessibility for updates/upgrades of the processes to accommodate new technologies (claim 29 – computer program product residing on computer readable medium; claim 30 – computer readable medium is ROM; claim 31 - computer readable medium is RAM; claim 33 – processor and memory are incorporated into single board computer).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of Cam through a processor running software from a read-only or random access memory in a single board computer. Implementations of methods and processes through software instructions residing on computer readable medium such as ROM and RAM can be much less expensive than hardware implementations and provide accessibility for updates/upgrades of the processes to accommodate new technologies.

5. Claims 4, 6, 7, 12, 13, 15, 16, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Bucholz et al. (US005440545A), hereafter Bucholz.

- In regards to Claims 4, 6, 12, 13, 15, 16, and 28,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam does not explicitly show storing a data element concerning the packet being processed, comprising a data packet length remainder indicative of the packet portion not fragmented and a packet truncation indicator indicative of incomplete fragmentation

of the packet, if another port contains an available packet, where the element allows subsequent process of the remainder of the data packet being processed in order to monitor and determine when the packet is fully fragmented.

Bucholz discloses a packet delivery system in which packets are fragmented for transmission (Title; Abstract). Referring to Fig. 6, Bucholz shows that a reassembly header (stored data element) is stored in the fragmented packet indicating its place within the packet, total packet length, total fragments, etc. such that it can be determined when the packet is fully fragmented (Col. 6-7, lines 63-23; claim 4,12 – storing data element concerning the packet being processed if another port contains an available packet, where the element allows subsequent process of the remainder of the data packet being processed; claim 13 – data packet length remainder indicative of packet portion not fragmented; claim 13 – packet truncation indicator indicative of incomplete fragmentation of the packet; claim 6,15,16,28 – monitoring and determining if the data packet has been fully fragmented).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam by storing a reassembly header for the packet currently being processed, including information regarding how much of the packet has been fragmented and how much remains, so that subsequent processing of the remainder of the packet fragments can be performed, as taught by Bucholz. This would enable the transmission system to recognize when a complete packet has been processed when transmitted in a number of fragments.

- In regards to Claim 7,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Referring to Fig. 5, Cam shows that polling of the PHY devices to determine if packets are available for processing is continuously done so that it is determined if any other ports contain packets available for processing other than those that have already so indicated (Col. 1, lines 38-41; Col. 3, lines 19-24; claim 7 – re-determining if packets are available for processing on any of the plurality of ports if the number of cells have been generated from the first port determined to have a packet available).

6. Claims 5, 8, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Bucholz as applied to claim 4 above, and further in view of Colmant et al. (US006144662A).

- In regards to Claims 5, 8, and 17,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam does not explicitly show initiating fragmentation on a data packet from another port while the fragmentation of the data packet on the first port continues until user-defined cells are generated.

Colmant discloses a non-blocking switch. Referring to Figs. 1B and 3B, Colmant shows that a packet received on a port 85 may be fragmented into several portions

(6001-6004) while another received packet on another port 85 may also be fragmented into portions (6125-6128), thereby enabling multiple port packet fragmentations to operate in parallel to keep, thereby improving the utilization of the transmission medium. the waiting time for a blocked output port low (Col. 9, lines 14-42; claim 5,8,17 – initiating fragmentation on a data packet from another port while the fragmentation of the data packet on the first port continues until user-defined cells are generated).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam to enable a received packet on another port proceed with fragmentation while the fragmentation of a first packet on the first port continues. By fragmenting received packets in parallel, processing delay required to fragment a packet prior to transmission could be eliminated.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Colmant.

In regards to Claim 14,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam does not explicitly show initiating fragmentation on a data packet from another port while the fragmentation of the data packet on the first port continues until user-defined cells are generated.

Colmant discloses a non-blocking switch. Referring to Figs. 1B and 3B, Colmant shows that a packet received on a port 85 may be fragmented into several portions (6001-6004) while another received packet on another port 85 may also be fragmented into portions (6125-6128), thereby enabling multiple port packet fragmentations to operate in parallel to keep, thereby improving the utilization of the transmission medium. the waiting time for a blocked output port low (Col. 9, lines 14-42; claim 14 – initiating fragmentation on a data packet from another port while the fragmentation of the data packet on the first port continues until user-defined cells are generated).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam to enable a received packet on another port proceed with fragmentation while the fragmentation of a first packet on the first port continues. By fragmenting received packets in parallel, processing delay required to fragment a packet prior to transmission could be eliminated

8. Claims 20-22 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Jha (US006847644B1).

- In regards to Claims 20-22 and 34,

Cam discloses a packet data transfer method on an interface having a large number of ports that covers all limitations of parent claim 9. (Abstract).

Referring to Fig. Cam shows that a Layer/master device 22 polls the PHY devices 14-20 to determine which have data waiting to be transferred (Col. 1, lines 38-41; claim 21 – determining which ports contain a data packet available for processing).

Cam shows that data packets waiting to be transferred from polled PHY devices are fragmented to a maximum block size (cell) of data. This maximum block size may be fixed at start-up or by programming through an external management interface (Col. 3, lines 2-9; claim 21 – fragmenting available data packet into at least one cell having defined size; claim 21 – fragmentation continues until a user-defined number of cells are generated; claim 22 – monitoring the number of cells produced to determine if user-defined number are generated).

Referring to Fig. 6, Cam further discloses that a selected PHY device transfers a block of fragmented packet data upon selection and deselects itself at the end of its transfer period, which is set at the specified maximum block size, and the next PHY with data to transmit is selected (Col. 12-13, lines 63-16).

Cam does not explicitly disclose the fragmentation process where a portion of a second available data packet on a different port is fragmented subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet.

However, referring to Figs. 5 and 11, Cam shows that packets awaiting transfer from multiple PHY devices will be transferred a maximum block size at a time before deselecting itself, at which point the next PHY device begins transfer of a maximum block size. In the situation where the PHY devices have large packets to be transferred,

a first portion of the packet on the first PHY will be fragmented and transferred, followed by a first portion of a second packet on the second PHY being fragmented and transferred. Subsequent portions of the first packet at the first PHY would be fragmented and transferred at its next selected transfer period (claim 21 - fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of Cam by fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet. Such an implementation would enable the method of Cam to process large packets at multiple PHY devices such that no one PHY device starves bandwidth from the other PHY devices.

Cam also does not explicitly show the plurality of ports connected to a synchronous optical network and the fragmentation process producing ATM cells. Cam also does not explicitly show a processor and memory of an ATM/POS processor for performing the method.

Jha discloses hybrid data transport over optical networks. Referring to Fig. 2 and 4, a switch's ports are connected to a SONET network. Jha shows that SONET data frames may be inverse-multiplexed (fragmented) into smaller bandwidth streams, such

as ATM cell streams (Col. 1-2, lines 58-6; claim 21 - plurality of ports connected to a synchronous optical network; claim 20,21 - fragmentation process producing ATM cells). Referring to Fig. 3, Jha also shows that processing of ATM and Packet-over-SONET can be accommodated through a single switch 102a/n (claim 34 – processor and memory are incorporated into ATM/POS processor).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of Cam through an ATM/POS processor such that the plurality of ports are connected to a SONET network and the fragmentation process produces ATM cells, as shown by Jha. This would enable the high bandwidth SONET frames to transport Ethernet over ATM using standard protocols, as shown by Jha (Fig. 2; Col. 2, lines 35-41).

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Jha as applied to claim 21 above, and further in view of Bucholz.

In regards to Claim 23,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam does not explicitly show monitoring and determining if the data packet has been fully fragmented.

Bucholz discloses a packet delivery system in which packets are fragmented for transmission (Title; Abstract). Referring to Fig. 6, Bucholz shows that a reassembly

header is stored in the fragmented packet indicating its place within the packet, total packet length, total fragments, etc. such that it can be determined when the packet is fully fragmented (Col. 6-7, lines 63-23; claim 23 – monitoring and determining if the data packet has been fully fragmented).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam by storing a reassembly header for the packet currently being processed, including information regarding how much of the packet has been fragmented and how much remains, so that subsequent processing of the remainder of the packet fragments can be performed, as taught by Bucholz. This would enable the transmission system to recognize when a complete packet has been processed when transmitted in a number of fragments.

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Muller et al. (US006105122A), hereafter Muller.

- In regards to Claim 25,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam shows that PHY device addresses may be segmented to achieve balance between efficient memory mapping and address decoding. Cam does not explicitly disclose an unbalanced port-loading condition as a port-switching event.

Muller discloses a switch configuration in a multi-node processing system that directs transmission messages between nodes in order to balance the load of the network (Col. 26-27, lines 61-5; claim 25 – port-switching event is an unbalanced port-loading condition).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the process of Cam by considering an unbalanced port-loading condition as a port-switching event, as shown by Muller. This would further prevent any one port in Cam from consuming a disproportionate amount of bandwidth from the other ports and improve network utilization and efficiency.

Response to Arguments

11. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Knight et al. (US006854025B2) discloses a DMA scheduling mechanism
- Quirke et al. (US006654370B1) discloses backplane synchronization in a distributed system with clock drift and transport delay

- Momirov (US006484209B1) discloses efficient path based forwarding and multicast forwarding
- Crow et al. (US006453357B1) discloses a method and system for processing fragments and their out-of-order delivery during address translation
- Woodward et al. (US006151318A) discloses a method and apparatus for encapsulating ATM cells in a broadband network
- Charny et al. (US006072772A) discloses a method for providing bandwidth and delay guarantees in a crossbar switch with speedup
- Bellaton et al. (US006026093A) discloses a mechanism for dispatching data units via a telecommunications network
- Ellis et al. (US005497371A) discloses a digital telecommunications link for efficiently transporting mixed classes of packets

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory B Sefcheck whose telephone number is 571-272-3098. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GBS
4-21-2005

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